In the Specification:

Please replace the paragraph beginning at page 2, line 1 and ending at page 2, line 15 with the following rewritten paragraph:

Summary of the Invention

~~The invention is directed to~~ In accordance with an aspect of the present invention, there is provided an apparatus for filtering and amplifying a received signal that includes a desired signal portion embedded in an interfering signal portion. The apparatus includes a plurality of complex filter/amplifier stages connected in sequence. Each of the stages has a complex filter for attenuating an interfering portion of the received signal relative to the desired portion of a signal received by the complex filter, a controlled amplifier which has set minimum gain K_{min} and maximum gain K_{max} for amplifying ~~the received signal~~ the desired signal portion and the interfering signal portion of the signal received from the complex filter, where K_{min} may be negative, and a control circuit. The control circuit controls the amplifier gain K where $K_{min} \leq K \leq K_{max}$ such that the controlled amplifier seeks to generate ~~an output signal having~~ the desired signal of the signal received from the complex filter, which has a projected amplitude level. The apparatus provides an output of the last state of the complex filter/amplifier as the desired signal of the received signal at a predetermined signal level at the apparatus output as a result of a combined gain of the controlled amplifiers of the plurality of the complex filter/amplifier stages.

In accordance with a further aspect of the present invention, there is provided an apparatus for filtering and amplifying a complex in-phase I and quadrature phase Q received signals. The apparatus includes a plurality of sequentially connected complex filter/amplifier stages, each stage having: complex filter means for attenuating an interfering portion relative to a desired portion of signals received by the complex filter means; and controlled amplifier means having set minimum gain K_{min} and maximum gain K_{max} for amplifying the

signals received from the complex filter means, the signal received from the complex filter means including an in-phase I signal and a quadrature phase Q signal. The controlled amplifier means includes: a first variable gain amplifier for amplifying the in-phase I signal; and a second variable gain amplifier for amplifying the quadrature phase Q signal. The apparatus includes control means for generating a gain control signal for controlling a gain K of the first and second amplifiers where $K_{min} \leq K \leq K_{max}$ such that the controlled amplifiers seek to generate output signals having a projected amplitude level. The control means includes: a first rectifier for receiving the output of the first variable amplifier to provide a first rectified signal; a second rectifier for receiving the output of the second variable amplifier to provide a second rectified signal; summing means for adding the first and the second rectified signals; and error amplifier means having a first input coupled to the summing means and a second input coupled to a projected amplitude level signal for producing the gain control signal.

In accordance with a further aspect of the present invention, there is provided an apparatus for filtering and amplifying a complex in-phase I and quadrature phase Q received signals. The apparatus includes a plurality of sequentially connected complex filter/amplifier stages, each stage having: complex filter means for attenuating an interfering portion relative to a desired portion of signals received by the complex filter means; and controlled amplifier means having set minimum gain K_{min} and maximum gain K_{max} for amplifying the signals received from the complex filter means, the signal received from the complex filter means including an in-phase I signal and a quadrature phase Q signal. The controlled amplifier means includes: a first variable gain amplifier for amplifying the in-phase I signal; and a second variable gain amplifier for amplifying the quadrature phase Q signal. The apparatus includes control means for generating a gain control signal for controlling a gain K of the first and second amplifiers where $K_{min} \leq K \leq K_{max}$ such that the controlled amplifiers seek to generate output signals having a projected amplitude level. The control means includes: a first rectifier for receiving the input of the first variable amplifier

to provide a first rectified signal; a second rectifier for receiving the input of the second variable amplifier to provide a second rectified signal; summing means for adding the first and the second rectified signals; and error amplifier means having a first input coupled to the summing means and a second input coupled to a projected amplitude level signal for producing the gain control signal.

In accordance with a further aspect of the present invention, there is provided an apparatus for filtering and amplifying a complex in-phase I and quadrature phase Q received signals. The apparatus includes a plurality of sequentially connected complex filter/amplifier stages, each stage having: complex filter means for attenuating an interfering portion relative to a desired portion of signals received by the complex filter means; and controlled amplifier means having set minimum gain K_{min} and maximum gain K_{max} for amplifying the signals received from the complex filter means, the signal received from the complex filter means including an in-phase I signal and a quadrature phase Q signal. The controlled amplifier means includes: a first variable gain amplifier for amplifying the in-phase I signal; and a second variable gain amplifier for amplifying the quadrature phase Q signal. The apparatus includes control means for generating a gain control signal for controlling a gain K of the first and second amplifiers where $K_{min} \leq K \leq K_{max}$ such that the controlled amplifiers seek to generate output signals having a projected amplitude level. The apparatus includes a received signal strength indicator having: gain summation means for receiving the gain control signal from each of the complex filter/amplifier stages for computing the overall gain of the apparatus; means for detecting and amplitude of the apparatus output signal; and means coupled to the gain summation means and the detector means for indicating the strength of a desired signal received by the apparatus.

The present invention is particularly advantageous in that the apparatus is capable of providing an overall output signal at a predetermined amplitude level within a restricted dynamic range from input signals having a wide variety of signal strengths and at the same time permits for the use of low power consuming subsequent circuits. This is achieved in apparatus that itself draws

very low power. The apparatus operates effectively on received signals in the IF band that are low-IF or zero-IF.

Please replace the paragraph beginning at page 4, line 1 and ending at page 4, line 5 with the following rewritten paragraph:

Figure 5b illustrates a quadrature feedforward AGC circuit in accordance with the present invention having DC feedforward compensation; [[and]]

Figure 6 illustrates a control circuit for the AGC's in accordance with the present invention [[.]]; and

Figure 7 illustrates an example of a received signal strength indicator (RSSI).

Please add the following paragraph at page 13, line 14:

Figure 7 illustrates an example of the RSSI 32 of Figure 2. The RSSI 32 of Figure 7 includes a gain summation circuit 70 for receiving gain control signals 72_1, 72_2, ..., 72_n from the complex filter/amplifier stages (e.g., 27_1, 27_2, ..., 27_n of Figure 2) for computing the overall gain of an apparatus (e.g., 20 of Figure 2). The RSSI 32 of Figure 7 further includes a detector 74 for detecting the amplitude of the output signal 76 of the apparatus. The RSSI 32 of Figure 7 further includes a circuit 78 coupled to the gain summation circuit 70 and the detector 74 for indicating the strength of a desired signal received by the apparatus. The gain control signals 72_1, 72_2, ..., 72_n may be the actual gains 31_1, 31_2, ..., 31_n of Figure 2 or the AGC setting gain control signals such as 15_1, 15_2, ..., 15_n of Figure 1, 30_1, 30_2, ..., 30_n of Figure 2.